REMARKS

Applicants respectfully request favorable reconsideration of this application, as amended.

An endorsed copy of Form PTO-1449 from the Second Supplemental Information Disclosure Statement dated October 1, 2003, is requested with the next official communication.

In the outstanding Office Action, all pending claims were allowed with the exception of Claims 51-58, which were rejected under 35 U.S.C. § 102(b) as being anticipated by Horiguchi et al. (Horiguchi). Without acceding to the rejection, each of Claims 51-56 has been amended to recite the arrangement of the logic gates with greater particularity, whereas Claims 57 and 58 have been amended more particularly to define the arrangement of the first and second pairs of potential lines. Applicants respectfully submit that, at least as presently amended, Claims 51-58 distinguish patentably from Horiguchi.

As amended, Claims 51-56 now recite that the first logic gate and said second logic gate each have two pairs of potential line portions, respectively including portions of the first pair of potential lines and portions of the second pair of potential lines, and further have a portion of at least one substrate potential line which supplies a

substrate potential. See, for example, Figs. 19(B)-21(B). This arrangement allows for the placement of the first and second logic gates in a common row with high density. Conventional logic gates, as per the arrangement shown in Fig. 19(A), have only one pair of power supply line portions (BDD and VSS in the figure). In order to place such conventional logic gates of different types (e.g. high-speed and low-speed) in a common row, it is necessary to provide a substantial interval between adjacent cells of different types in order to avoid short circuiting of power lines. This increases chip size as well as the length of a signal line between the two different cells, with a corresponding increase in signal propagation delay.

Horiguchi fails to teach or suggest an arrangement of first and second logic gates as defined in Claims 51-56 discussed above. Accordingly, Claims 51-56 distinguish patentably from Horiguchi.

Claim 57 has been amended additionally to recite that the second mask pattern includes a figure pattern for forming the first pair of potential lines and the second pair of potential lines in parallel in one row pattern. Claim 57 is therefore believed to be allowable in view of the indication of allowability of Claim 60.

Claim 58 has been amended to recite that the description of the first logic gate and the description of the second logic have the first pair of potential lines and the second pair of potential lines in common. Claim 58 is therefore believed to be allowable in view of the indication of allowability of Claim 61.

Notwithstanding the previous indication of allowability, a number of the allowed claims have been amended along similar lines to those discussed in connection with Claims 51-58 in order to conform with the subject matter intended to be claimed in the present application at this time. Claims 60 and 61 have been cancelled, as the present amendments effectively incorporate their subject matter into Claims 37 and 38, respectively.

In view of the amendments and remarks presented hereinabove, this application is believed to be in condition for allowance.

The Commissioner is hereby authorized to charge to Deposit Account No. 50-1165 any fees under 37 C.F.R. §§ 1.16 and 1.17 that may be required by this paper and to credit any overpayment to that Account. If any extension of time is required in connection with the filing of this

paper and has not been requested separately, such extension is hereby requested.

Respectfully submitted,

By: _____
Mitchell W. Shapiro
Reg. No. 31,568

MWS:sjk

Miles & Stockbridge P.C.
1751 Pinnacle Drive
Suite 500
McLean, Virginia 22102
(703) 903-9000

December 18, 2003